WHAT IS CLAIMED IS:

1. A strained Silicon FinFET (Fin Field Effect Transistor), comprising:

a substrate;

a strained silicon in a shape of a fin island located on said substrate;

a semiconductor embedded in said strained silicon;

a dielectric layer formed on a surface of an intermediate section of said strained silicon; and

electrodes formed on said fin island and said dielectric layer.

2. The strained Silicon FinFET as claimed in claim 1, wherein said substrate is an SOI (Silicon on Insulator) substrate.
3. The strained Silicon FinFET as claimed in claim 1, wherein said semiconductor is employed for generating a strained silicon channel.
4. The strained Silicon FinFET as claimed in claim 1, wherein said semiconductor is selected from a group consisting of a SiGe alloy, a SiGeC alloy, a SiC alloy, and a material which is suitable for producing strained silicon.
5. The strained Silicon FinFET as claimed in claim 1, wherein said surfaces of said intermediate section of said strained silicon covered by said dielectric layer comprise left side, right side, and top side surfaces of said intermediate section.
6. The strained Silicon FinFET as claimed in claim 1, wherein said dielectric layer is one of an oxide layer and a high dielectric constant (high K) layer.
7. The strained Silicon FinFET as claimed in claim 6, wherein said high dielectric constant (high K) layer is selected from a group consisting of HfO_2, Si_3N_4, and Al_2O_3.
8. The strained Silicon FinFET as claimed in claim 1, wherein said electrodes

are a gate electrode formed on a surface of said dielectric layer, a source electrode formed on one terminal of said strained silicon; and a drain electrode formed on the other terminal of said strained silicon.

9. The strained Silicon FinFET as claimed in claim 7, wherein said gate electrode is selected from a group consisting of an n^+ doped polysilicon gate electrode, a p^+ doped polysilicon gate electrode, an n^+ doped poly SiGe gate electrode, a p^+ doped poly SiGe gate electrode, and a metal gate electrode.
10. The strained Silicon FinFET as claimed in claim 1, wherein said strained silicon has conducting carriers.
11. The strained Silicon FinFET as claimed in claim 10, wherein said conducting carrier is one of an electron and a hole.
12. A method for manufacturing a strained Silicon FinFET, comprising:
    (a) providing a substrate comprising a first silicon layer thereon;
    (b) forming a semiconductor layer on said substrate;
    (c) forming a fin-shaped island;
    (d) forming a second silicon layer on a surface of said fin-shaped island;
    (e) forming a dielectric layer on surfaces of said second silicon layer at an intermediate section of said fin-shaped island; and
    (f) forming electrodes on said dielectric layer and said fin-shaped island.
13. The method for manufacturing the strained Silicon FinFET as claimed in claim 12, wherein said substrate is an SOI (Silicon on Insulator) substrate.
14. The method for manufacturing the strained Silicon FinFET as claimed in claim 12, wherein said semiconductor is employed for generating a strained silicon channel.

15. The method for manufacturing the strained Silicon FinFET as claimed in claim 12, wherein said semiconductor is selected from a group consisting of a SiGe alloy, a SiGeC alloy, a SiC alloy and a material which is suitable for producing strained silicon.

16. The method for manufacturing the strained Silicon FinFET as claimed in claim 12, wherein said fin-shaped island comprises said semiconductor layer and said first silicon layer.

17. The method for manufacturing the strained Silicon FinFET as claimed in claim 12, wherein the method for forming the fin-shaped island is etching.

18. The method for manufacturing the strained Silicon FinFET as claimed in claim 12, wherein said surface of said fin-shaped island covered by said second silicon layer is the whole surface of said fin-shaped island.

19. The method for manufacturing the strained Silicon FinFET as claimed in claim 12, wherein said dielectric layer is one of an oxide layer and a high dielectric constant (high K) layer.

20. The method for manufacturing the strained Silicon FinFET as claimed in claim 19, wherein said high dielectric constant (high K) layer is selected from a group consisting of HfO_2, Si_3N_4, and Al_2O_3.

21. The method for manufacturing the strained Silicon FinFET as claimed in claim 12, wherein said surfaces of said second silicon layer covered by said dielectric layer comprise left side, right side, and top side surfaces of said second silicon layer.

22. The method for manufacturing the strained Silicon FinFET as claimed in claim 12, wherein said electrodes are a gate electrode formed on a surface of said dielectric layer, a source electrode formed on one terminal of said strained silicon; and a drain electrode formed on the other terminal of said

strained silicon.

23. The method for manufacturing the strained Silicon FinFET as claimed in claim 22, wherein said gate electrode is selected from a group consisting of an n^+ doped polysilicon gate electrode, a p^+ doped polysilicon gate electrode, an n^+ doped poly SiGe gate electrode, a p^+ doped poly SiGe gate electrode, and a metal gate electrode.